Publications

Timm Bostelmann

March 11, 2024

[1] Julian Weihe, Timm Bostelmann, and Sergei Sawitzki. Processing speed impact of the pipeline-length on a custom RISC-V CPU for FPGAs. In *The Fifteenth International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS)*, pages 5–8, October 2022.

[2] Tobias Thiemann, Timm Bostelmann, and Sergei Sawitzki. Improving the gradient descent based FPGA-placement algorithm. In *The Thirteenth International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS)*, pages 12–24, November 2020.

[3] Timm Bostelmann, Tobias Thiemann, and Sergei Sawitzki. Fast FPGA-placement using a gradient descent based algorithm. *International Journal On Advances in Systems and Measurements*, 13(1 & 2):175–184, 2020.

[4] Timm Bostelmann, Tobias Thiemann, and Sergei Sawitzki. Accelerating FPGA-placement with a gradient descent based algorithm. In *The Twelfth International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS)*, pages 13–18, October 2019.

[5] Thomas Fabian Starke, Timm Bostelmann, and Sergei Sawitzki. FPGA-basierter protein- und DNA-sequenzvergleich zur optimierten datenbanksuche mit dem BLAST-algorithmus. In *M. Eibl, M. Gaedke (Hrsg.):INFORMATIK 2017, Lecture Notes in Informatics (LNI), Gesellschaft für Informatik*, pages 469–480, September 2017.

[6] Timm Bostelmann, Thomas Fabian Starke, and Sergei Sawitzki. Local alignment search in genetic sequences on a low-cost fpga. In *The Tenth International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS)*, pages 39–43, September 2017.

[7] Thomas Fabian Starke, Timm Bostelmann, Helga Karafiat, and Sergei Sawitzki. A synthesizable VHDL export for the custom architecture design tool CustArD. In *The Tenth International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS)*, pages 44–48, September 2017.

[8] Timm Bostelmann, Philipp Kewisch, Lennart Bublies, and Sergei Sawitzki. Improving FPGA-placement with a self-organizing map accelerated by GPU-computing. *International Journal On Advances in Systems and Measurements*, 10(1 & 2):45–55, 2017.

[9] Timm Bostelmann and Sergei Sawitzki. Improving the performance of a SOM-based FPGA-placement-algorithm using SIMD-hardware. In *The Ninth International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS)*, pages 13–15, July 2016.

[10] Timm Bostelmann and Sergei Sawitzki. Ein Entwurfsfluss für die geführte Optimierung rekonfigurierbarer Architekturen. In *DASS 2016 - Tagungsband Dresdner Arbeitstagung Schaltungs- und Systementwurf*, pages 47–50, Mai 2016.

[11] Timm Bostelmann and Sergei Sawitzki. A heterogeneous architecture template for application domain specific reconfigurable logic. In *2015 Austrian Workshop on Microelectronics (Austrochip)*, pages 9–14, September 2015. IEEE.

[12] Timm Bostelmann and Sergei Sawitzki. Towards a guided design flow for heterogeneous reconfigurable architectures. In *International Conference on Field Programmable Logic and Applications (FPL)*, pages 23–24, September 2015. IEEE.

[13] Timm Bostelmann and Sergei Sawitzki. A conceptual toolchain for an application domain specific reconfigurable logic architecture. In *International Conference on Reconfigurable Computing and FPGAs (ReConFig)*, pages 1–4, December 2014. IEEE.

[14] Hanno Sternberg, Timm Bostelmann, and Sergei Sawitzki. CustArD - a custom architecture design tool. In *International Conference on Reconfigurable Computing and FPGAs (ReConFig)*, December 2014. IEEE.

[15] Timm Bostelmann and Sergei Sawitzki. Improving FPGA placement with a self-organizing map. In *International Conference on Reconfigurable Computing and FPGAs (ReConFig)*, pages 1–6, December 2013. IEEE.

[16] Timm Bostelmann and Sergei Sawitzki. Einsetzbarkeit selbstorganisierender Karten für die Platzierung von Netzlisten. In *DASS 2013 - Tagungsband Dresdner Arbeitstagung Schaltungs- und Systementwurf*, pages 56–61, April 2013.

[17] Timm Bostelmann and Sergei Sawitzki. Automatische und teilautomatische Generierung anwendungsspezifischer Beschleunigungshardware aus der Softwarebeschreibung. In *DASS 2011 - Tagungsband Dresdner Arbeitstagung Schaltungs- und Systementwurf*, pages 108–113, Mai 2011.